The Design of Switchmode Converters Above 100 kHz

by Rudy Severns

With the introduction of power MOS switches, and the general improvement in other components, it is now possible to design switchmode converters with switching rates in the range of 100 kHz to 5 MHz, and from both off-line and low voltage DC bases.

Unfortunately, a 200 kHz switchmode converter is a bit more than just a higher frequency version of the conventional 20 kHz converter. While the circuits and components used are similar, there are a host of significant differents which alter the design.

HOW HIGH IN FREQUENCY?

Early in the design process, a decision must be made on the switching frequency. Most performance parameters (cost, volume, bandwidth, efficiency, etc.) change rather slowly with increasing frequency, so there is relatively little to be gained by going up by a factor of two or three. If significant improvements are to be achieved, the switching frequency must be increased enough to not only reduce the size of the magnetic components, but also to enable the use of alternate components and materials which provide lower cost, improved performance or both. Real changes do not appear until the switching frequency has been increased by an order of magnitude or more.

The choice of operating frequency is influenced by the converter specification, the choice of switch (bipolar or MOSFET) and the power level. For offline switchers using bipolar switches, the optimum frequency would be about 200 kHz. From low voltage DC sources, the switching frequencies using bipolar devices can be increased to 300 to 600 kHz. If power MOSFET switches are used, the switching frequencies may be increased to the megahertz range, and there is increasing evidence that this may be desirable, for low power at least. As the power level goes below 100 watts, less and less is gained from operating around 200 kHz, the reason being that the components don't really get much smaller or cheaper. If real improvements are to be made at low power, new designs should operate in the low MHz region using air core magnetics and MOSFET switches. Fortunately, the lower the power level the easier it is to go up in frequency. As the output power is increased above 1KW, when using bipolar switches it will be necessary to reduce the switching frequency towards 100 kHz because the available large devices are somewhat slower. As large power MOSFET's become available, higher frequency operation will be possible.

CIRCUIT TOPOLOGY

Having chosen a switching frequency, the next step is to select circuit topology. While the common 20 kHz converter topologies (parallel, half-bridge, full bridge, etc.) can be used at 200 kHz, the performance can be a good deal less than optimum.

As shown in Figure 1, the converter can be viewed as having primary and secondary topologies connected by a transformer. Because of the difficulties of designing the power transformer at 200 kHz, each of the three circuit elements must be considered in relation to the other two. For example, the incorrect selection of primary switch or output rectifier connection may make the transformer impractical at 200 kHz.

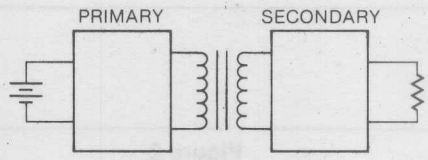

Figure 1.

For primary topologies, the designer must chose between switchmode (modified square waves) or resonant converters. If switchmode is desired, then the choice is between voltage-fed, current-fed with non-overlapping switch conduction, or current-fed with overlapping switch conduction. Table I is a comparison, pro and con for these options.

A variety of resonant circuits are available [1,2,3,4] to the designer but, except for the work by Miller, these circuits have not yet been widely used at high frequencies. Thus, it is difficult to comment on their use from direct experience. From a theoretical point of view, however, the resonant converters should work very well indeed, and if it is possible to operate the current-fed switchmode circuits in the resonant mode by adding a resonating capacitor, then a large number of new resonant converter topologies will be available to the designer. It is also possible that some of the series and parallel commutated SCR inverter circuits can be used as high frequency resonant converters, with power MOSFETs instead of SCRs as switches. The use of resonant converters, at high frequencies, deserves a good deal more attention than is being given at present.

Examples of good and poor choices for high frequency circuit topologies are shown in Figures 2 and 3. Figure 2 is a current-fed circuit; [5] Figure 3 is the common voltage-fed bridge quasi-squarewave converter. A comparison of the two circuits is given in Table II. In general, the current-fed family of converters is more suitable for high frequency switchmode converters.

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Table I. Regulator Topology Tradeoffs

PRO	CON
Voltage Fed Converter 1. Wide Variety of Circuits 2. Good Output Regulation at Heavy Loads 3. Circuit Well Understool	1. Current Spikes can be severe 2. Switch Overlap is Fatal 3. Capacitive Losses Poor at Low Powers 4. Poor Output Regulation at Light Loads 5. Poor EMI Characteristics 6. High Switch Transition Stress
Current Fed Converter 1. Wide Variety of Circuits 2. No Current Spikes 3. Storage Time Overlap OK 4. Good Multiple-Output Regulation at All Loads	1. Voltage Spikes 2. Capacitive Losses Poor at Low Power 3. Moderate EMI Characteristics 4. Moderate Switch Transition Stress
Resonant Converter 1. Low Switching Transition Stresses 2. Low Capacitive Loss 3. Low EMI	1. Resonating Capacitors a Problem 2. Q Multiplication Increases Currents or Voltages 3. Fixed Frequency Operation Presents Problems 4. Circuits Tend to be More Complex

Table II. Circuit Comparisons

Figure 2	Figure 3
1. Even with fast recovery diodes, the reverse recovery time of the output rectifiers, is a significant portion of the operating cycle. D1 will be in forward conduction while D2 is still recovering. This places a short circuit across the secondary which is reflected into the primary. Because this circuit is current-fed, the only effect is to slightly increase the energy stored in L1 preventing current spiking in the switches.	1. During the rectifier reverse recovery time, a current spike is reflected into the primary switches. At 200 kHz, the transformer leakage inductance is made quite small by design, so there is very little impedance to limit the current spike. If Schottky barrier diodes are used, the large diode capacitance will also cause primary current spikes.
2. Using the full wave rectifier shown, the output rectifier reverse voltage will be twice the output voltage plus one diode drop (not including noise), irrespective of the line voltage, so that hot carrier diodes can be used at voltages above 5 volts.	2. For a given output voltage, the diode reverse voltage is relatively high. As an example, with a 5 volt output and a 2:1 line excursion, the rectifier reverse voltage varies from 11.7 to 22.8 volts. If the switch storage time reduces the maximum ON time to prevent overlap, the reverse voltage is even higher. The higher reverse voltage also increases the dV/dt that the rectifier is subjected to.
3. At high frequencies, there is a greater tendency towards primary volt-second asymmetry, especially if bipolar switches are used. This can cause core saturation current spikes in voltage fed topologies. In this circuit, spiking is prevented by L1, and core saturation is relatively harmless. Current spikes due to reflected capacity and switch overlap, are also suppressed.	3. There is no protection from core saturation, switch overlap or reflected winding capacitance current spikes. In the case of bipolar switches, the need to prevent overlap due to storage time, allowing for manufacturing and temperature variations, can significantly reduce the pulse width dynamic range. Core saturation can be reduced by inserting a series capacitor in the primary, but this capacitor must be carefully selected to prevent core saturation during fast line or load slewing.
4. Because a single choke is common to all outputs, cross regulation between the outputs for varying loads is relatively good.	4. Separate chokes are required on each output, and for good regulation each choke must remain in continuous conduction. There is no compensation for the choke resistive regulation effects. The net result is that at 200 kHz, the cross regulation of multiple outputs is poor.
5. Diodes D3 and D4 do not see a reverse potential at the end of their conduction cycle, so the reverse recovery time of these devices is not critical.	

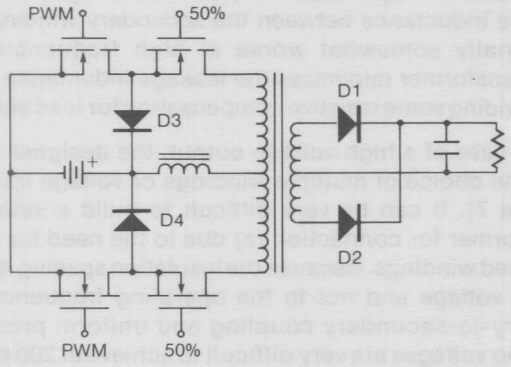


Figure 2.

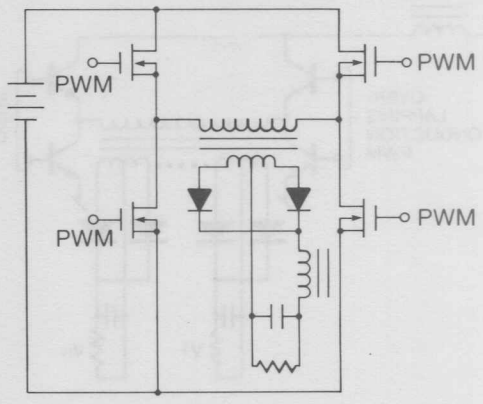
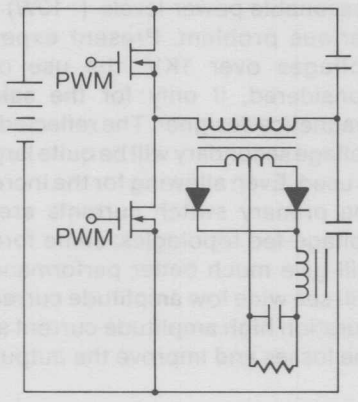
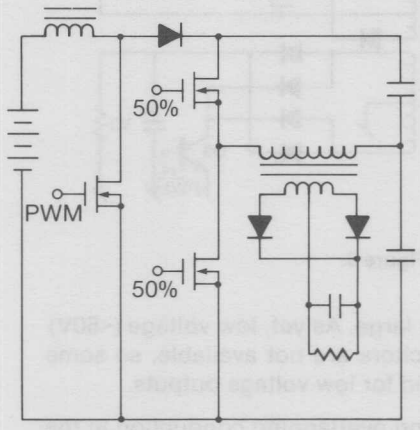


Figure 3. Quasi-Squarewave Converter





Half-Bridge

Low Line, P_T = 35.8W
High Line, P_T = 12.9W
T_j = 122°C

(A)

Boost Regulator/Half-Bridge

Low Line, P_T = 9.1W
High Line, P_T = 6.5W
T_j = 63°C

(B)

Figure 4.

Not only the switching frequency, but the choice of switch can affect the choice of topology. For example, if power MOSFETs are used as switches, the topology selected can have a profound effect on the conduction losses. A simple example is shown in Figure 4. Figure 4(a) is a normal half-bridge quasi-squarewave converter, while 4(b) is an unmodulated half-brdige preceeded by a boost regulator. Given the conditions in Table III, the power losses for (b) are much lower than (a). Because the cost of power MOSFETs is a strong function of $1/r_{DS}$, the three devices used in (b) may be much cheaper than the two devices in (a). While this is a fairly simple example, the boost derived family of converters generally provides lower MOSFET conduction losses than buck derived current-fed converters. Figure 5(a) and (b) shows two examples of boost derived current-fed converters, one using overlapping conduction and the other a secondary shunt switch. There are many other possible circuits[6] that may be used. Unfortunately, the boost family of converters has disadvantages also:

1. The control loop transfer function contains a right half-plane zero which is difficult to compensate for with single loop feedback. By using multiple AC and DC loops, this problem can be overcome.
2. The output ripple current in a boost converter is discontinuous (the input current is continuous) so that the

Table III. Power MOS Topology Conduction Loss Comparison Assumptions

1. P_O	= 200W
2. η	= 80% Without Switch Losses
3. V_{DC}	= 200V to 375V
4. T_A	= 50°C
5. r_{DS}	= 2.5Ω at 25°C
6. Filter Inductor is Large	
7. BV_{DSS}	= 450V to 500V
8. θJ_A	= 4°C/W (TO-3 Case and Heat Sink)
9. r_{DS}	Temperature Coefficient is 0.6%/°C

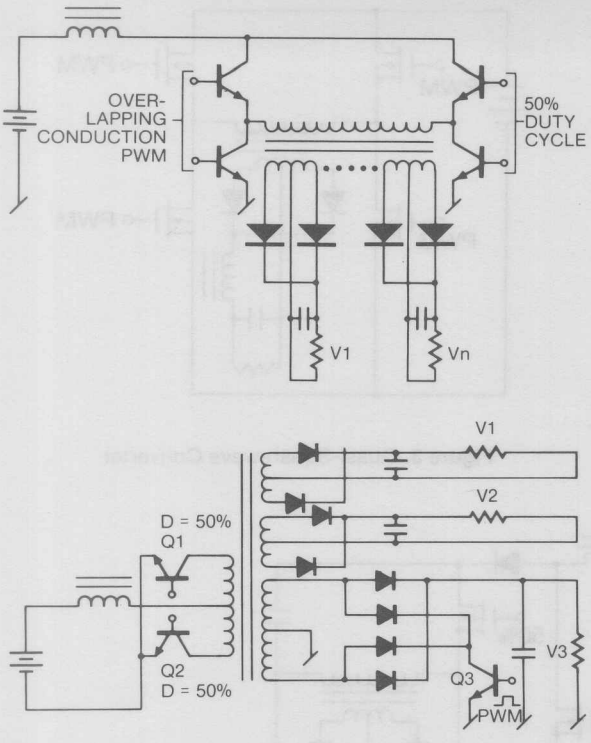


Figure 5.

output ripple current is large. As yet, low voltage (<50V) high current film capacitors are not available, so some penalty in volume is paid for low voltage outputs.

3. In those converters using overlapping conduction in the primary, a large voltage spike can be generated due to the interruption in the primary by secondary leakage inductance current. When the shunt switch is in the secondary, this spiking is greatly reduced.

The output winding/rectifier topology must also be carefully selected with an eye to transformer limitations and primary topology requirements. Figure 6 shows two rectifier connections for multiple outputs. In (a), separate windings are used, and in (b), an autotransformer connection is used. If DC isolation between outputs is not required, then the connection

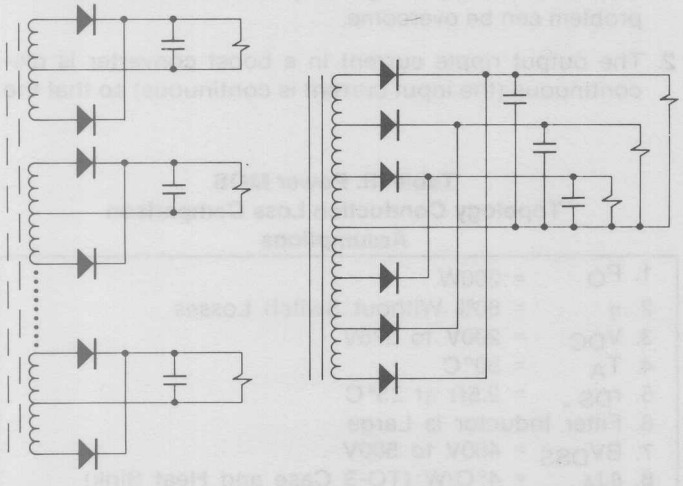


Figure 6.

in (b) should be used because it will give much better cross regulation. A major cause of poor cross regulation is the leakage inductance between the secondary windings, proportionally somewhat worse at high frequencies. The autotransformer minimizes the leakage inductance, as well as providing some resistive compensation for load variations.

In the case of a high voltage output, the designer is faced with the choice of multiple windings or voltage multipliers (Figure 7). It can be very difficult to build a satisfactory transformer for connection (a) due to the need for stacked insulated windings. Because the insulation spacing is related to the voltage and not to the operating frequency, good primary-to-secondary coupling and uniform predictable winding voltages are very difficult to achieve at 200 kHz. The voltage multiplier makes the transformer design easier, but requires a large number of capacitors. Fortunately at 200 kHz, these capacitors can be quite small. The diode shunt capacity is the most serious limitation for high frequency multipliers, but for small multiplication ratios (3 to 5) and reasonable power levels (>10W) this does not seem to be a serious problem. Present experience indicates that for voltages over 1KV, the use of multipliers should be considered, if only for the sake of the sanity of your magnetics designer. The reflected capacitance from the high voltage secondary will be quite large, especially if a multiplier is used. Even allowing for the increased leakage inductance, the primary switch currents are usually unacceptable in voltage-fed topologies; some form of current-fed topology will give much better performance. The voltage multiplier will see wide low amplitude current pulses rather than short duration high amplitude current spikes, and this will reduce the losses and improve the output regulation.

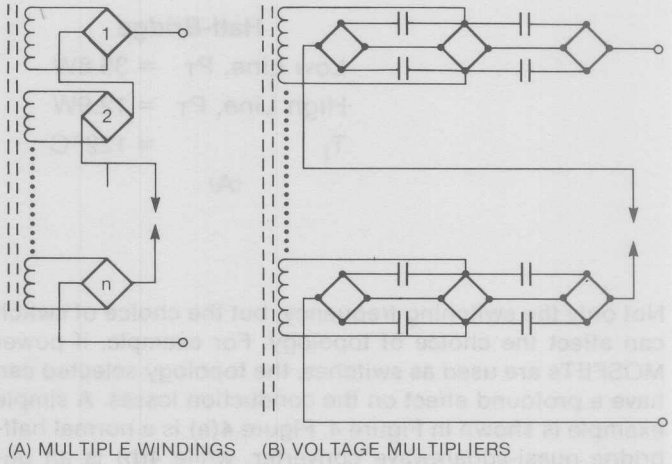


Figure 7. HV Rectifier Schemes

FEEDBACK LOOP CONSIDERATIONS

Increasing the switching frequency from 20 to 200 kHz provides a similar increase in the feedback loop gain cross-over frequency. Given the proper type of control loop and compensation, a gain cross-over of 20 to 100 kHz is possible, comparable to the usual series regulator. While it is possible for the designer to put in a single low frequency pole with gain cross-over at 1 to 2 kHz and have performance equal to a 20 kHz switcher, most designers will opt for higher bandwidth. As with the input and output topologies, the feedback scheme must be carefully considered. Table IV is a

Table IV. Fixed Frequency Control Options

1. Single DC Loop 2. DC Loop and Switch Peak Current Control
3. DC Loop and Choke Voltage Sensing
4. Feed Forward

PRO	CON
Single DC Loop 1. Well Understood 2. Simple Control Circuits 3. For 20 kHz Equivalent Performance a Single Low Frequency Pole May be Used	1. Moving Capacitor ESR Zero Uncompensated 2. Variable Load Capacity is Uncompensated 3. Load Capacity May be Much Larger than IC Filter Requirements 4. Two-Pole Rolloff with Peaking 5. Boost Converters have Right Half-Plane Zero 6. Gain Crossover Limited to 10-15% of f_O 7. No Inherent Current Limiting
DC Loop and Switch Peak Current 1. Inherent Overcurrent Protection 2. Inherent Soft Start Capability 3. Higher Gain Crossover Frequency 4. Single Pole Rolloff 5. Inherent Current Sharing for Parallel Modules	1. More Complex Control Circuit 2. Requires Switch Current Sensor 3. No Compensation for Moving ESR Zero 4. No Compensation for Varying Load Capacity
DC Loop and Inductor Voltage Sense 1. Higher Gain Crossover Frequency 2. Right Half-Plane Zero Compensation 3. Compensation for Variable Load Capacitance 4. Moving ESR Zero Compensation 5. Single Pole Rolloff	1. Complex Control Circuit 2. Choke Voltage Sensor Required 3. No Inherent Current Limiting
Feed Forward 1. Very Simple in DC Loop Systems 2. Compensates for Loop Gain Variation with Duty Cycle 3. Improves Line Transient Response	1. Difficult to Apply to Multiloop Systems 2. Not Adequate as Regulation Loop by Itself

comparison of the more common fixed frequency control schemes.

A number of control problems may be encountered at high frequencies. AT 20 kHz, the output filter capacitor is usually selected for low ESR, with capacitance a secondary consideration. Usually the filter capacitor is large, compared to the load capacitance. However at 200 kHz, the film capacitors used have an ESR two orders of magnitude smaller, so the filter capacitor will now be much smaller and the load capacity may very well be larger than the filter capacitor. The load capacitance may also be undefined or variable. This can make it very difficult to stabilize the feedback loop. If power modules are to be paralleled, each loop sees the capacity of the other modules, which may also be a variable. When a boost-derived topology is used, there is a right half-plane zero in the control transfer function.

These effects cannot easily be compensated for in the simple DC control loop. Much better performance can be obtained if a combination of AC and DC loops are used. [7,8,9] The use of multiple loop control schemes is highly recommended above 100 kHz.

Some other control loop gremlins which appear at high frequencies are:

1. The circuit stray capacitance is proportionately larger at 200 kHz, so there is an increased likelihood of sub-harmonic instabilities due to capacitive feed-through at the ripple frequency. Careful layout and good bypassing are the best means to combat this problem.
2. In some types of pulse width controller circuits, the time delay in the digital elements (especailly if CMOS is used) may become large enough to cause significant phase shift due to transport delay. As a rough guide, the delay times though the controller should be kept below 5% of the half-period, or about 100 nsec in a 200 kHz converter.

COMPONENTS AT HIGH FREQUENCIES

Operation with switching rates above 100 kHz requires a fresh look at component selection. As in the case of the circuit topology, each of the circuit components must be evaluated for performance, taking into account component parasitic effects which are often ignored at 20 kHz.

Switches

The designer has the choice of using either bipolar or MOSFET devices; some of the tradeoffs are given in Table V. As MOSFETs become less expensive and more diverse in ratings, there is little question that power MOSFETs will be the switch to use above 100 kHz, but at present, bipolars must be considered for some applications with suitable circuit arrangements to compensate for performance limitations.

Fast switching times in bipolars can be achieved by first selecting fast devices and then driving them correctly. The switching time test circuits used by bipolar manufacturers often do not drive the device ON or OFF hard enough, so that the publicized switching times are often not truly indicative of the devices' capabilities. The gain bandwidth, f_t, when given, is a much more reliable indicator of usefulness at high frequencies. Generally, the designer should select devices with an f_t of 10 mHz or more, and then test the devices in the actual circuit. Figure 8 shows an idealized base current drive waveform. At turn-on, a large, fast-rising current pulse is applied. When the device is fully ON, the turn-on pulse is removed and sufficient base drive, in proportion to I_C if possible, is provided to keep the switch in or near saturation. At turn-off, a fast rising negative current pulse is applied to minimize the storage time. A large turn-off pulse will also produce a rapid fall time in low voltage devices and very fast high voltage devices using interdigated structures. It has been shown,[15] however, that for many high voltage transistors, a large turn-off pulse, while reducing the storage time, may extend the turn-off current tail, significantly increasing the switching loss. For devices rated at 400 volts and higher, it may be desirable to use a more gradually decreasing base drive and exchange increased storage time for reduced switching losses. During the OFF time, the base of the transitor should be clamped to the emitter through a low impedance; this will minimize false turn-on due to noise and capacitive coupled currents induced by high dV/dt in other parts of the circuit. These requirements are really not difficult to meet and a wide variety of circuits are possible.[10] Figure 9 shows several possibilities using the DS0026 clock driver as a basis. This IC will source and sink 1A in <20 nsec, and provides an excellent interface between the logic and the switch drive. The IC may be used barefoot, as in (a) and (c) or with power MOSFETs, as in (b). To reduce the storage time, some form of antisaturation circuit can be employed to prevent the collector voltage from going below the base. The Baker Clamp (Figure 10) is perhaps the simplest and most common way to accomplish this. It provides a marked reduction in storage time, but does not really improve the transition times in fast low voltage devices. In a high voltage device, where a good deal of charge is stored in the collecter region during saturated operation, the use of a clamp will reduce the turn-off transition time. It should be kept in mind that there is a limit to the useful turn-off beyond which there is no further improvement. Excessive negative base drive during reversed bias operation causes current crowding in the emitter region, which in turn lowers the threshold at which secondary breakdown will occur. The designer should provide sufficient drive to obtain good performance, but no more.

As the base is driven harder, some devices (especially high voltage transistors) will display a region of quasi-saturation at turn-on, as shown in Figure 11. Low voltage devices, and those using an interdigitated structure display this effect to a lesser extent. Unfortunately, the data sheet is seldom of much help in determining the presence of this problem and the designer may be forced to test a number of different types of devices in his circuit to find out which are suitable and which are not. In a similar manner, quasi-saturation and a current tail can occur at turn-off,[11] and again, the only way at present to detect these effects is by testing. Table VI is a short summary of bipolar performance limits.

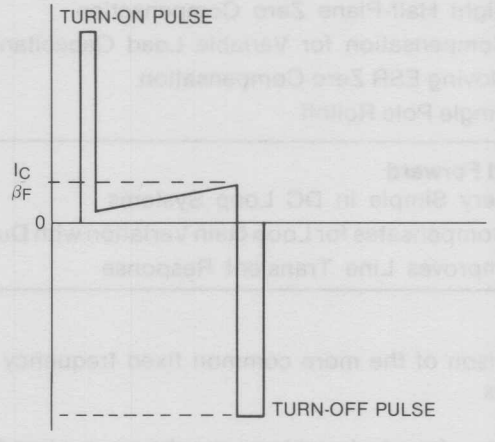


Figure 8. Ideal Bipolar Base Drive

Table V. MOSFET Versus Bipolar Tradeoffs

MOSFET	BIPOLAR
1. FET switches are much faster - 10 to 20 nsec switching times can be readily achieved.	1. Transition times of 50 to 200 nsec at best, with careful base drive design.
2. No storage time effect.	2. Storage times of 500 to 1500 nsec common. This can be reduced to 150 to 300 nssec with antisaturation circuits.
3. Very low drive power required.	3. Base drive requirements relatively high, especially with base overdrive for fast switching.
4. MOSFETs are more expensive at present, but should be much cheaper in the future.	4. At present bipolars, even fast ones, are lower in cost.
5. There is limited selection of MOSFET power devices.	5. A very wide variety of high speed and high power devices are available.

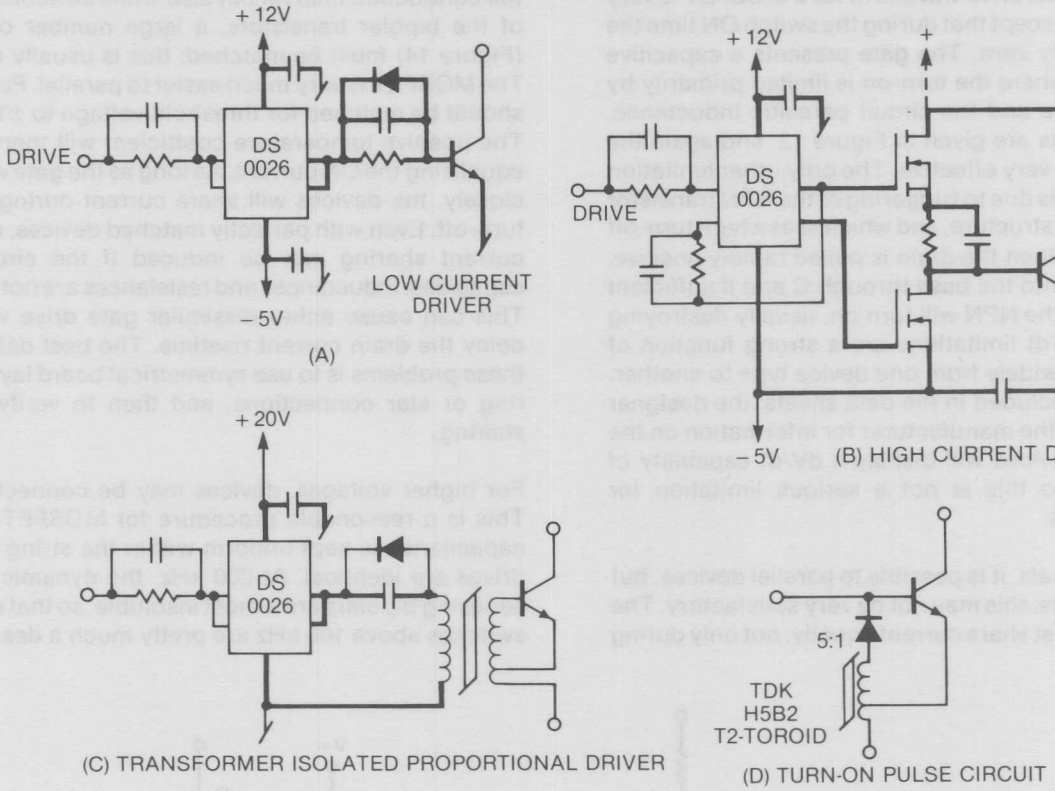


Figure 9. High frequency Base Drive Circuits

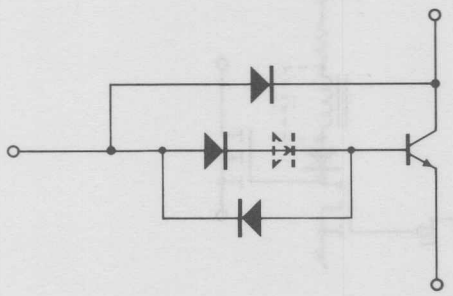


Figure 10. Storage Time Reduction Circuit (Baker Clamp)

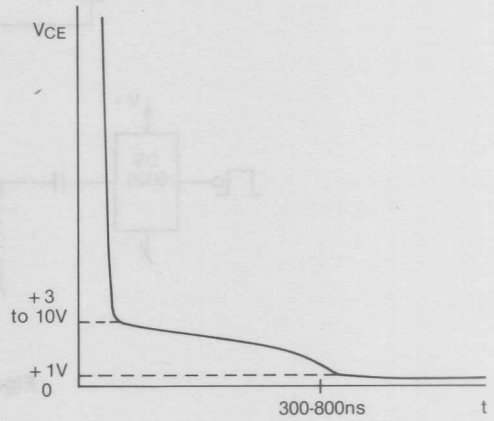


Figure 11. Bipolar Turn-on Plateau

Table VI. Typical Bipolar Performance Limits

PART	V_{CEO}	I_C	t_r	t_f	t_s	f_t
2N5330	140V	20A	50ns	30ns	300ns	20MHz
2N6280	140V	50A	60ns	60ns	400ns / 70ns Clamped	30MHz
2N6590	450V	10A	60ns	100ns	400ns	40MHz
D62T	500V	100A	150ns	150ns	800ns Clamped	10MHz
GSDS 50020	200V	50A	100ns	100ns	400ns	?

The ideal gate current drive waveform for a MOSFET is very similar to a bipolar except that during the switch ON time the current is essentially zero. The gate presents a capacitive load to the driver, where the turn-on is limited primarily by the driver resistance and the circuit parasitic inductance. Several drive circuits are given in Figure 12, and again the MOS clock driver is very effective. The only other limitation on switching speed is due to triggering of the NPN transistor inherent in the MOS structure, and which sees a high turn-off dV/dt (Figure 13). When the drain is pulled rapidly positive, current is injected into the base through C and if sufficient current is injected, the NPN will turn on, usually destroying the device. The dV/dt limitations are a strong function of geometry and vary widely from one device type to another. Until such data is included in the data sheets, the designer will have to contact the manufacturer for information on the limitations. Most devices will display a dV/dt capability of 10V/ns or more, so this is not a serious limitation for switching regulators.

For higher power levels, it is possible to parallel devices, but in the case of bipolars, this may not be very satisfactory. The parallel switches must share current equally, not only during the conduction interval but also while switching. In the case of the bipolar transistors, a large number of parameters (Figure 14) must be matched; this is usually not practical. The MOSFET is very much easier to parallel. Parallel devices should be matched for threshold voltage to ±10% or better. The positive temperature coefficient will then take care of equalizing the ON current. As long as the gate voltages track closely, the devices will share current during turn-on and turn-off. Even with perfectly matched devices, asymmetrical current sharing can be induced if the circuit parasitic capacities, inductances and resistances are not symmetrical. This can cause either dissimilar gate drive waveforms or delay the drain current risetime. The best defense against these problems is to use symmetrical board layouts, such as ring or star connections, and then to verify the current sharing.

For higher voltages, devices may be connected in series. This is a reasonable procedure for MOSFETs if the stray capacitance is kept uniform within the string and the gate drives are identical. At 200 kHz, the dynamic problems of seriesing bipolars are almost insoluble, so that series bipolar switches above 100 kHz are pretty much a dead issue.

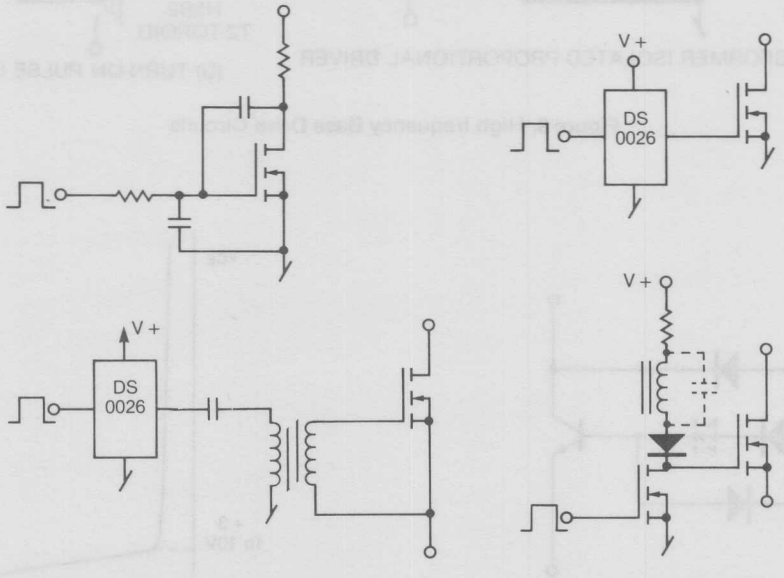


Figure 12. VMOS Drive Circuits

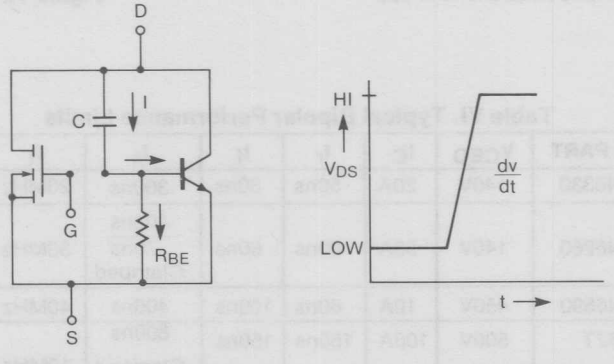
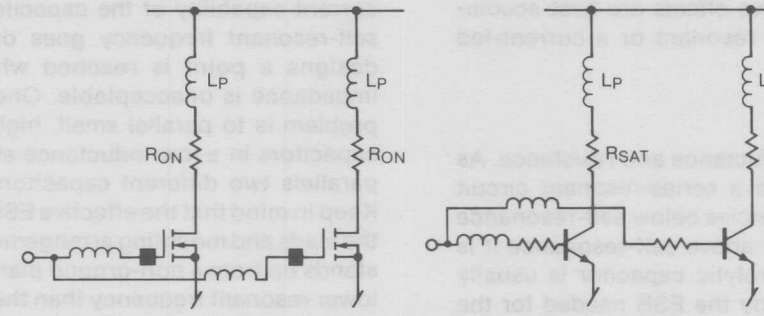


Figure 13. Parasitic NPN Switchback



(A) MATCHING REQUIREMENTS

1. Vgs(th)
2. DRIVE CURRENT

(B) MATCHING REQUIREMENTS

1. STORAGE TIME
2. V_{CESAT}
3. RISE AND FALL TIMES
4. DRIVE CURRENT

Figure 14. Parallel Switch Connections

Junction Diodes

Above 100 kHz, the dominant diode limitation is reverse recovery time, t_{rr}. For efficient rectification the devices selected should have a t_{rr} less than 100 ns, although 200 ns devices can be used if the power loss is acceptable. The need for speed limits the selection to either gold doped devices, such as those manufactured by TRW, Semtech, and Unitrode, or the ion-implanted diodes, produced by SSDI. Table VII is a short summary of present performance limits. Each of the manufacturers has a good variety of devices, so that other than the price penalty, adequate diodes are available. Some manufacturers have indicated that if a large quantity demand were present, most of the cost premium could be eliminated. If the circuit subjects the diodes to a fast rising current waveform, a turn-on voltage spike (Figure 15) across the diode may be observed. This spike has two causes. First the package inductance, and second, the finite time required for the diode to go into full conduction. This is referred to as the forward recovery time, t_{fr}, and is present in most gold-doped devices to some extent. The major effect of t_{fr} is to cause voltage spikes to appear in the circuit, which can stress both the switches and the other rectifiers. As in the case of some bipolar effects, the data sheets are no help and the designer may have to try several devices to obtain one that is suitable.

Diodes can be paralled for high current operation, but in addition to matching the V_F characteristics, careful balancing of the parasitic inductance and resistance is needed. Figure 16 illustrates this point. Again, symmetry of layout is needed, as well as symetrical winding within the transformer. The multiple transformer windings must have equal resistance and be distributed within the transformer, so that equal voltages are induced in each winding.

Table VII. Typical Diode Performance Limits

MANUFACTURER	Type	V_R	I_F	t_{rr}
UNITRODE	UES803	150V	70A	50ns
TRW	SVD450-12	450V	12A	70ns
SEMTECH	3FF500	50V	1A	30ns
TRW	DSR5100	1000V	4A	100ns
SSDI	HSR4S	150V	20A	25ns

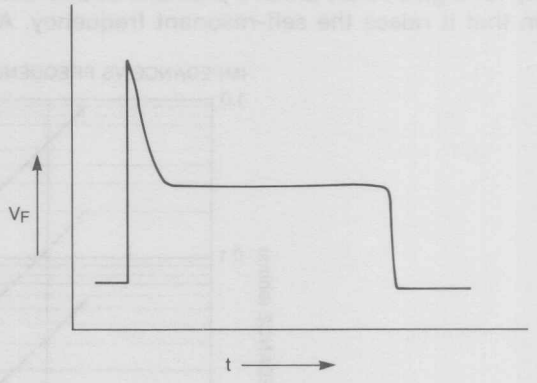


Figure 15. Silicon Junction Diode Forward Recovery Spike

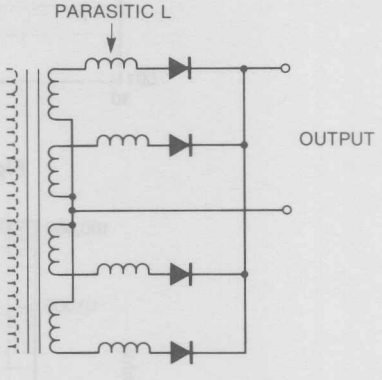


Figure 16. Parallel Diodes

Schottky Barrier Diodes

For low voltages and high currents, the Schottky barrier diode is well suited for high frequency operation. However there are some problems: even though t_{rr} is very short, the large junction capacitance creates circuit effects that are barely distinguishable from t_{rr} problems. There are also dV/dt limitations. Schottky barrier diodes are limited to a dV/dt of 0.7V/ns, and require the use of snubbers to limit the dV/dt. Snubbers are good practice in any case, to limit

voltage transients. The capacitive effects are best accommodated for by using either a resonant or a current-fed topology.

Capacitors

All capacitors have parasitic inductance and resistance. As shown in Figure 17, this forms a series-resonant circuit (usually low Q) so that at frequencies below self-resonance the capacitor is capacitive, and above self-resonance it is inductive. At 20 kHz and electrolytic capacitor is usually used with the size determined by the ESR needed for the ripple current. The result is that the filter capacity is much larger than required to obtain low ESR. The large capacitance makes the self-resonant frequency very low; a typical example is shown in Figure 18. The ESR of an electrolytic capacitor does not vary greatly above 20 kHz, so that its size, for a given ripple current, is essentially independent of frequency. For this reason, either plastic film or ceramic capacitors are used at high frequencies where the ESR of a good film capacitor may be two orders of magnitude less than the best electrolytic, (Figure 19). At 200 kHz the smaller capacity for a given ESR is not a problem, and in fact is an asset in that it raises the self-resonant frequency. As the current capability of the capacitor increases however, the self-resonant frequency goes down, and in high power designs a point is reached where the high frequency impedance is unacceptable. One circuit trick to beat this problem is to parallel small, high self-resonant-frequency capacitors in a low inductance structure. Another scheme parallels two different capacitors as shown in Figure 20. Keep in mind that the effective ESL of the capacitor includes the leads and mounting arrangement, so that a capacitor that stands up from a non-ground plane board may have a much lower resonant frequency than the same capacitor mounted close on a ground plane board with minimum lead lengths and the outer foil grounded to the ground plane. When small values of capacity are needed, ceramic capacitors can be used effectively, however not all ceramic dielectrics have low losses, particularly those with the highest K, so some care must be exercised in selecting ceramic capacitors.

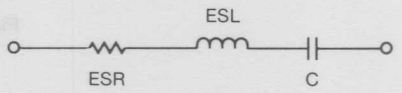


Figure 17. Capacitor AC Equivalent Circuit

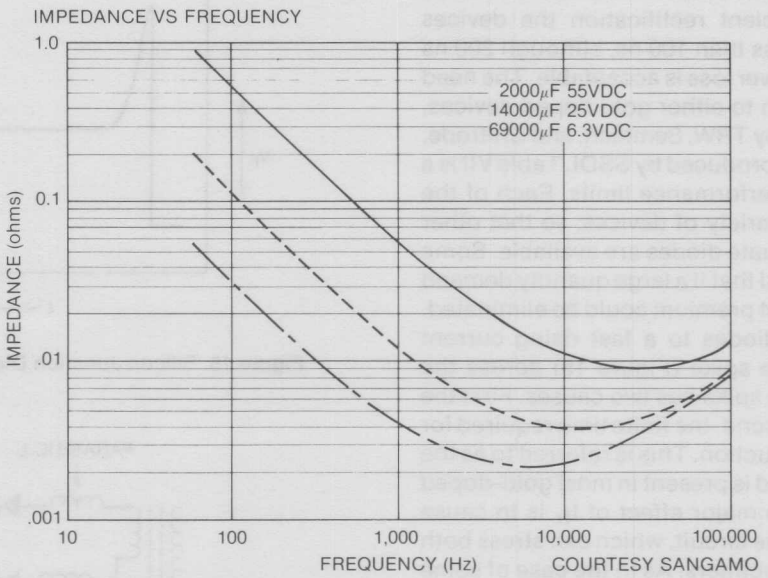


Figure 18. Electrolytic Capacitor Impedance

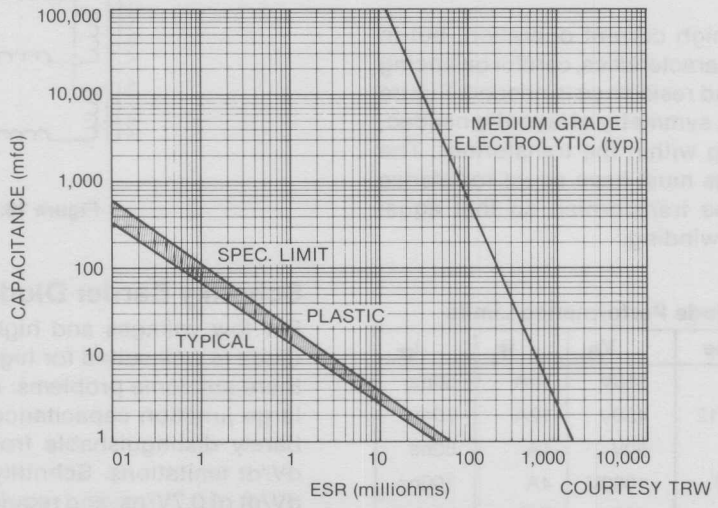


Figure 19. Plastic Film Versus Electrolytic

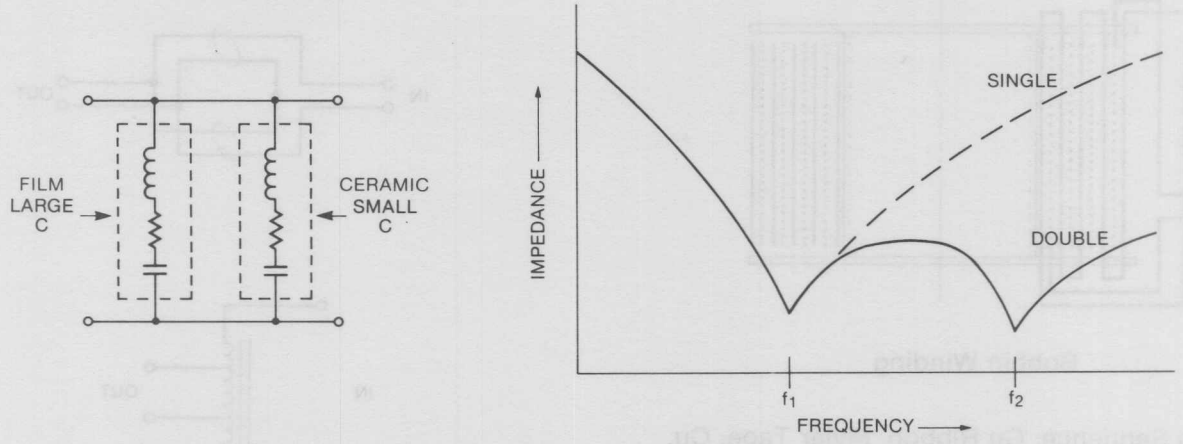


Figure 20. Compound Capactior

High Frequency Magnetics

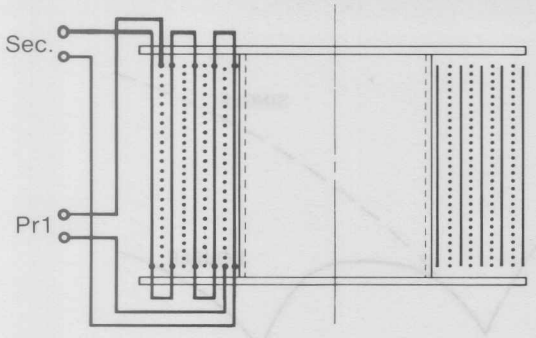
The high frequency power transformer is usually the most difficult component in a high frequency switcher. While a number of satisfactory solutions have been found, this is clearly an area where a great deal more work is necessary.

Most of the common core materials, such as ferrites, powdered iron, tape cores and perhaps amorphous metals can be used at 200 kHz as long as the flux density is restricted for acceptable self-heating. The first choice for a transformer core would be a ferrite such as Ferroxcube 3C8 or Mag-Inc F material. If either the mechanical or temperature environments preclude the use of ferrites, a thin (½ mil) tape core can be used if the flux density is kept low. For chokes, powdered iron toroids are very useful. At 20 kHz, the low μ of powdered iron, as opposed to molypermalloy, makes it relatively unattractive, but at 200 kHz, this is not a problem and the core cost for powdered iron is about 10% of molypermalloy. There appear to be no special advantages to any particular core shape (cup cores, E/I, toroids, etc.) at high frequencies. Because of the reduced number of turns used, however, most cores have too much window for the core area, so that the proportions of all the shapes are not really optimum. An expensive cure is to go to custom cores, but, hopefully, as more designers go to high frequencies, the manufacturers will create new standard sizes for this application.

The high frequency magnetics can be wound with standard magenetic wire, but much better copper utilization can be achieved if Litz, multifilar magnet wire or copper ribbon is used. The reason for this is that the skin effect becomes very pronounced above 100 kHz (and lower at high powers!). Litz and multifilar magnet wire use the principle that the smaller the wire gauge the greater the copper utilization, so that a number of parallel small wires will have a lower AC resistance that the same amount of copper in one wire. Litz wire is essentially multifilar magnet wire that has been braided to further equalize the current distribution. The additional cost of Litz wire is balanced by the very small amounts that are typically used. The only significant problem with Litz wire is stripping the large number of small wires to make connections.

The greatest ingenuity is required in the winding of the transformer to reduce the leakage inductance, and to produce symmetrical and predictable voltages in the output windings. The first step would be to interleave layers of primary and secondary (Figure 21). Better coupling can be had if the primary and secondary are wound multifilar in each layer (Figure 22a). Even better coupling can be had if the primary and secondary are wound of twisted or co-axial transmission lines (Figure 22b). This is the principle of RF transmission line transformers, as shown in Figure 23, 24, 25 and 26. A 1KW 200 kHz version of Figure 25 has been built with a turns ratio of 31:1, the leakage inductance as seen from the 31 turn primary was 1.9 μHy. In a true RF transmission line transformer, the source and load impedances are directly related to the winding characteristic impedance so that tremendous bandwidth is possible. This kind of impedance matching is not very practical for switching regulators, nevertheless, mismatched co-axial transformers are still relatively wide band. Some improvement can be gained by cascading an RF transformer with a conventional transformer (Figure 27) to reduce the turns ratio in the isolation transformer. The RF transformer is usually a very simple and inexpensive structure.

Inductors display parallel self-resonance (Figure 28) due to the winding capacity. The self-resonant frequency must be kept well above the ripple frequency to provide adequate filtering action. A high resonant frequency can be achieved by reducing the winding capacity as much as possible; there are a number of ways to do this: single layer with spaced turns, bank winding, maintaining a large gap between the ends of the winding and minimizing the winding to core capacity by wrapping the core with a low K dielectric. There is a limit, however, to how high the self-resonant frequency can be pushed and it is usually necessary to use a multisection filter such as shown in Figure 29. To avoid complicating the feedback loop compensation, the additional poles should be above gain crossover and well damped. If ferrite beads are used for the high frequency portion of the filter, these requirements are usually met.



Bobbin Winding

Winding Sequence: Cu Ribbon, Mylar Tape, Cu, Mylar, Litzwire, Mylar, Cu, Mylar, Cu

Figure 21. High Frequency Transformers

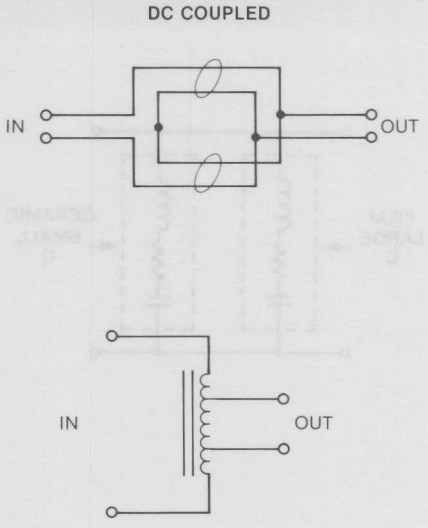


Figure 23. Transmission Line Transformers

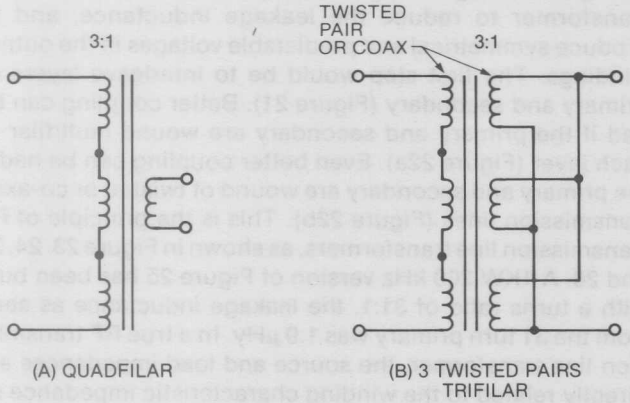


Figure 22. High Frequency Transformer Winding Techniques

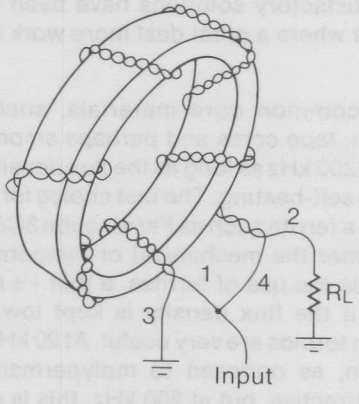


Figure 24. Transmission Line Transformer

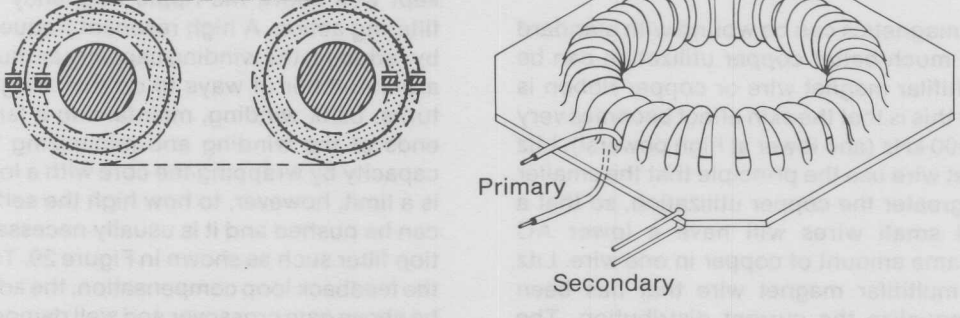


Figure 25. Coaxial Wound Toroid

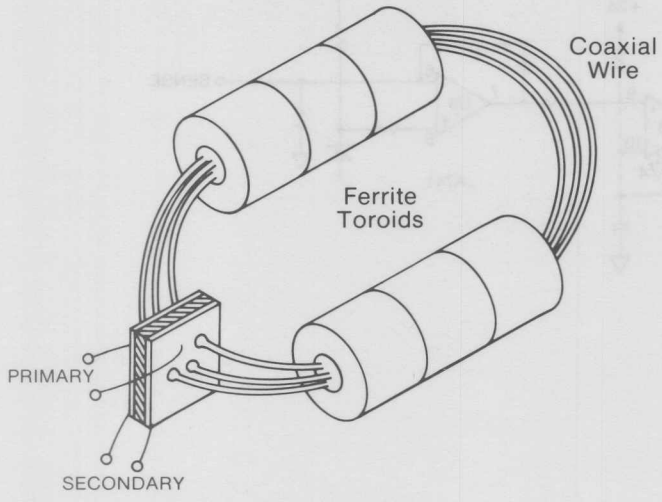


Figure 26. RF Transformer

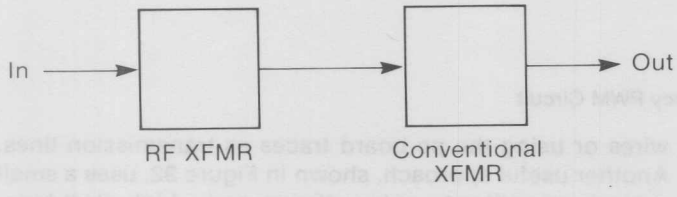


Figure 27. RF Transformer Used to Reduce Turns Ratio in Conventional Transformer

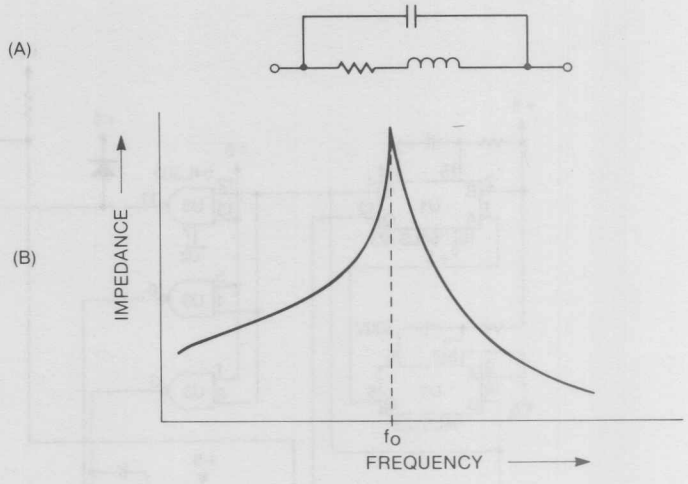


Figure 28. Inductor Self Resonance

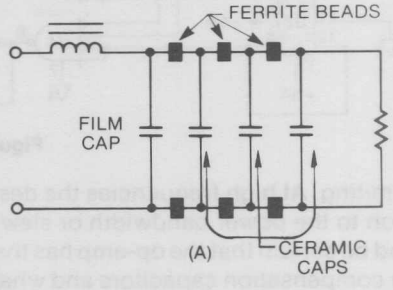


Figure 29. High Frequency Output Filters

Integrated Circuits

A wide variety of Ic op-amps, comparators, pulsewidth modulators and drivers, is available to the 20 kHz switcher designer, but as the frequency is raised to 200 kHz the ranks thin out, especially amoung pulse width modulator IC's.

There are several limitations on the present crop of IC modulators:

1. Limited operating frequency. The majority of IC's have maximum oscillator frequencies of 100 kHz. A few will run at 300 kHz, and one is good up to 500 kHz. Keeping in mind that a push-pull converter will run at one-half the oscillator frequency, this limits the operating frequency to 50 to 150 kHz, except when using the Ferranti IC.
2. Lack of source/sink output drivers. Most IC's do not provide for both source and sink capability at high current levels. This is needed to provide proper drive for power MOSFETs and bipolar transistors.
3. Insufficient drive current. None of the present IC's can supply the ±500 mA current pulses required to switch high voltage power MOSFETs quickly.
4. Slow output transitions. Even in the 500 kHz modulator, the output switch transition can be >100 ns, much too slow for 200 kHz switches.
5. Excessive minimum dead time. The typical minimum dead time is 500 ns. At 200 kHz this is 20% of the half period and is a serious reduction in the available dynamic range.

The most satisfactory of the present IC's are the new Silicon General SG1526 and the Ferranti ZN1066.

The designer may very well have to build his own modulator using logic IC's. An example of a three hundred kHz PWM circuit is shown in Figure 30. U1 is two one-shots connected as an asymmetrical oscillator that produces a train of 100 ns pulses for timing, U2 is the output pulse steering flip-flop, U3 is an open collector gate used to generate the ramp, the comparator is U5, and U6 is the error amplifier. U4 and the remainder of U3 are used for gating and inhibit functions. The 54/74LS series of logic gives adequate speed with reasonable power consumption.

The following limitations exist when using op-amps:

1. Limited bandwidth. Many op-amps, especially the economical quads, have open loop bandwidths of 1 mHz or less. If the amplifier is operated with a gain of 10, then a pole will appear in the transfer function at 100 kHz or less. With gain crossover at 1 or 2 kHz, this is no problem, but if, in a 200 kHz switcher gain crossover is moved up to 20 to 50 kHz, compensation is made more difficult. Also, the common mode noise rejection capabilities of the op-amp are greatly reduced.
2. Subharmonic oscillations. By using op-amps that have high gain at high frequencies, there is an increased tendency towards subharmonic oscillation. This type of oscillation is manifested by alternating pulses of different length, usually at the one-half subharmonic, and is usually caused by capacitive ripple voltage feedback through the feedback amplifier. Because wideband op-amps are needed, this problem is best solved by shielding, capacitor bypassing right at the pins of the op-amp and careful attention to the board trace layouts to minimize capacitive pickup.

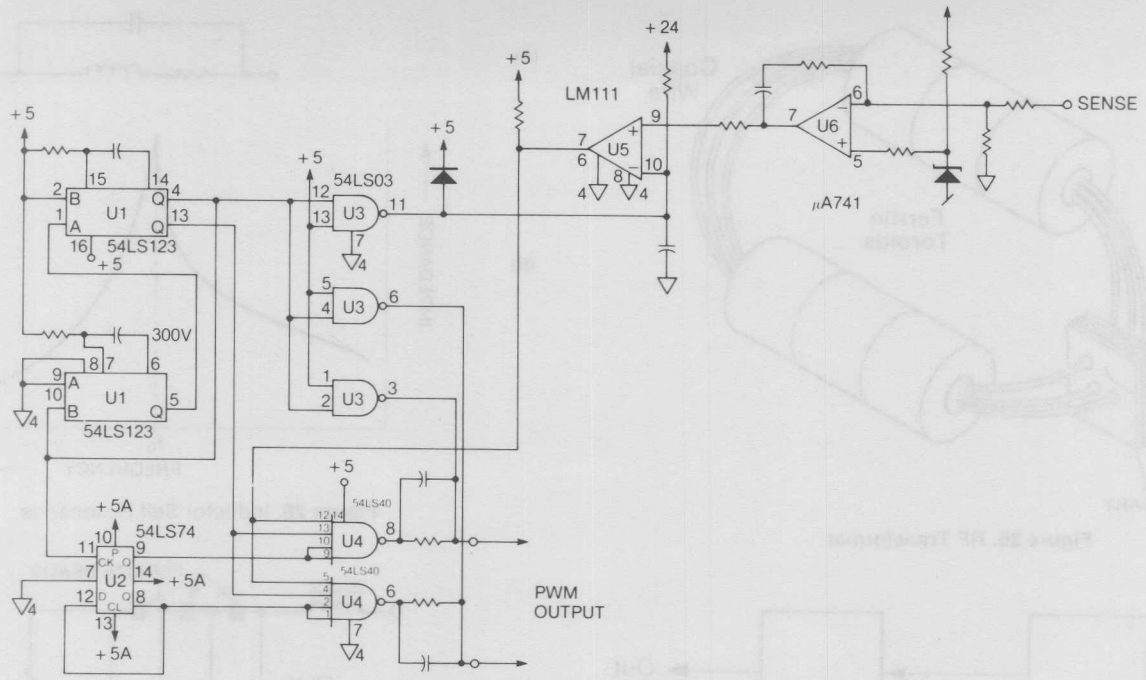


Figure 30. High Frequency PWM Circuit

3. Slew rate limiting. At high frequencies the designer must pay attention to the power bandwidth or slew rate of the op-amp, and be certain that the op-amp has the capability to drive the compensation capacitors and whatever other load is on the output of the op-amp.

Since comparator transitions of less than 100 ns are needed, most comparator IC's are eliminated; the LM111A is about as slow a comparator as is useful. Remember that the comparator switching speed is affected by the dV/dt of the input ramp, and the maximum practical ramp amplitude should be used to maximize dV/dt.

CIRCUIT LAYOUT

Having selected the circuit topology and the components, the designer is faced with putting it all together in a workable layout. At 20 kHz much latitude is permitted, and even the worst rats nest will work. This is *not* the case at 200 kHz. A 200 kHz switcher has frequency components beyond 100 mHz and has much more in common with a wideband RF amplifier than a 20 kHz switcher. A careless layout may very well not work at all. The key is "THINK RF" during the layout. A collection of useful layout tips are given in Table VIII. Figure 31 gives a good idea of how much inductance is introduced by the interconnection leads, and how this inductance can be reduced by either twisting the connecting wires or using the pc board traces as transmission lines. Another useful approach, shown in Figure 32, uses a small ceramic capacitor to reduce the area of a high dI/dt loop. This is simply an example of RF bypassing.

The final layout will probably look quite different from the 20 kHz norm but there is no reason that it need be exotic or any more expensive. In fact, due to the additional care used, it may very well be less expensive.

Table VIII. Circuit Layout Tips

1. Identify the Hi dI/dt Paths and Minimize their impedance
2. Minimize the Area of Current Loops
3. Use Twisted Leads for Transformer Connections
4. Arrange Transformer Lead Breakouts to Minimize Inter Connection Inductance
5. Bypass Hi dI/dt Loops with Ceramic Capacitors
6. Use Star or Ring Connections for Parallel Components
7. Use Goundplane Construction
8. Beware of Inductive Device Cases

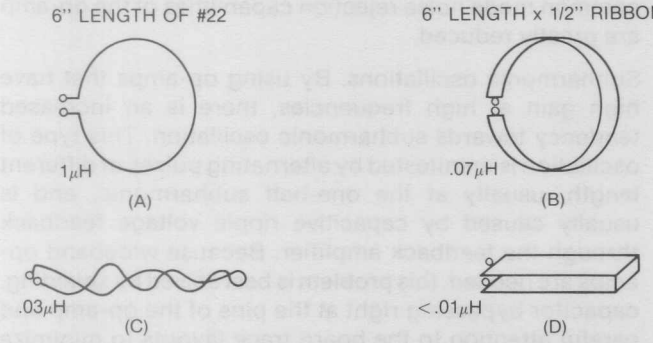


Figure 31. Inductance of Wire Loops

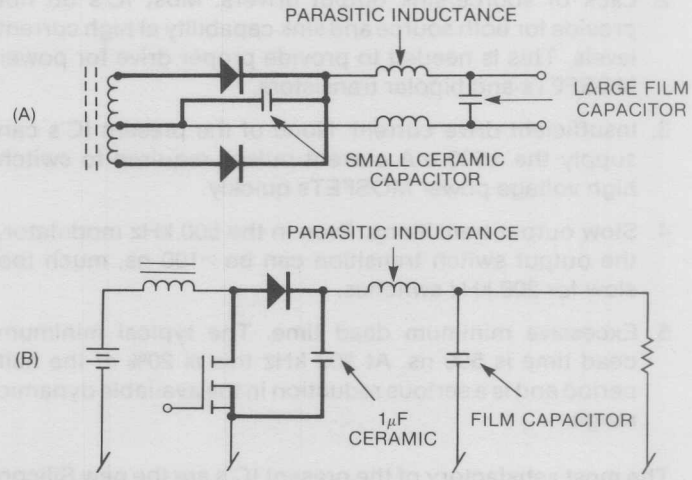


Figure 32. HF Bypassing

DESIGN EXAMPLES

1. 600kHz INVERTER

The initial investigation into a high frequency inverter was motivated by a requirement for a 600kHz sonar transducer driver. Lower frequency (50kHz) transducers were being driven by squarewave inverters, but the 600kHz transducers were being driven by class-B RF amplifiers with low efficiencies. Figure 1 is a schematic of the output section of the inverter that was designed for this purpose. The collector waveforms for a 100W (the circuit was tested to 150W) resistive load are given in Figures 2, 3, 4 and 5. As can be seen in Figure 5, the quality of the output waveform is excellent (the discontinuity in the middle of the rise and fall is a small deadband in the drive). The rise time is 40ns. It is interesting to note that the stray inductance inherent in the circuit is sufficient to delay the current rise so there is no turn-on loss. Turn-on times of 10-15ns were achievable. The turn-off time is about 100ns. The measured efficiency for this circuit was 92%, despite of the high switching frequency. The reason for this high efficiency is that the switch losses are moderate (a summary is given in Table 1), and the other circuit losses are quite small. The output transformer is a 11mm ferrite pot core (Mag. Inc. F Material), which was expected to work well at these frequencies. Surprisingly, however, a 0.5 mil supermalloy tape core also worked very well.

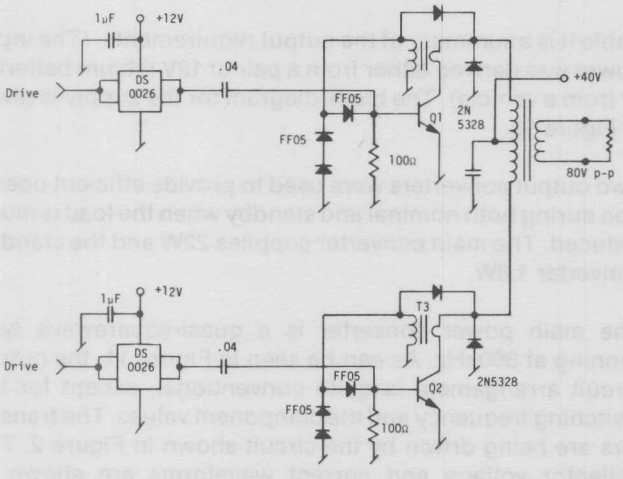


Figure 1. 600kHz Sonar Driver Output Circuit

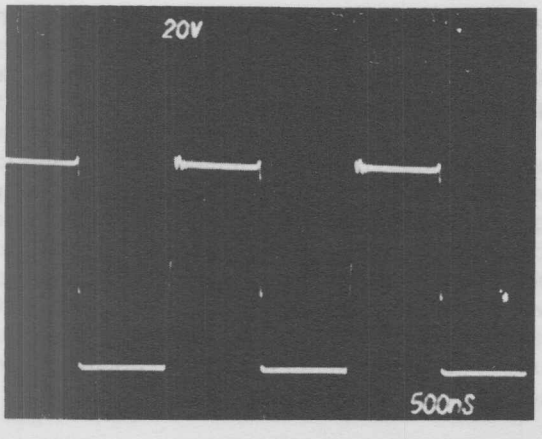


Figure 2. Q1 Collector Voltage

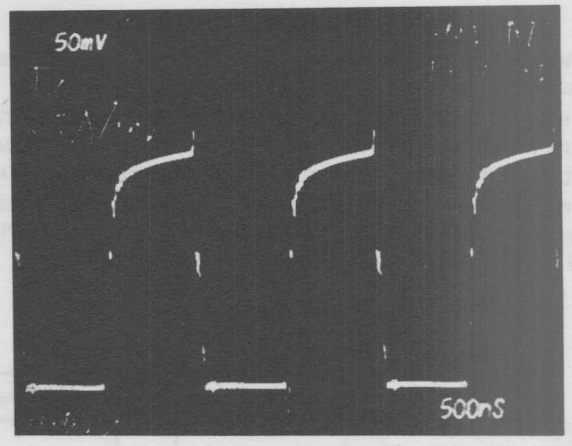


Figure 3. Q1 Collector Current

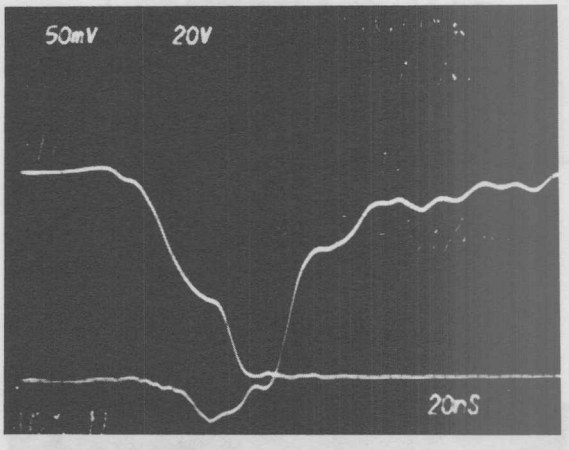


Figure 4. Q1 Turn-On Transition

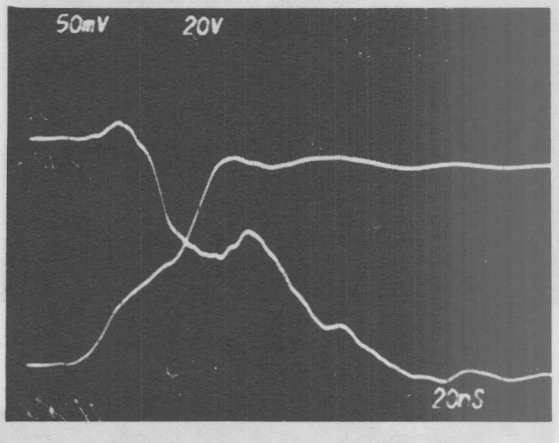


Figure 5. Q1 Turn-Off Transition

Table I
600 kHz Switching Loss Summary

Loss Mechanism	Power Loss
Turn-On Transition	0
Turn-Off Transition	3.0W
Collector Saturation	1.6W
Base Drive	.4W
TOTAL	5.0W

2. A 300kHz Boost Regulator

The next development was a 200W, 300kHz boost converter shown in Figure 6. A more complex drive scheme was attempted to further improve performance but was found to be only marginally worthwhile. Figures 7, 8 and 9, show the collector voltage and current waveforms. Rise time is 100ns, fall time 70ns and storage time 80ns. The largest switching loss was at turn-off (=5W). The overall efficiency was 90% for a 22V input and a 50V output.

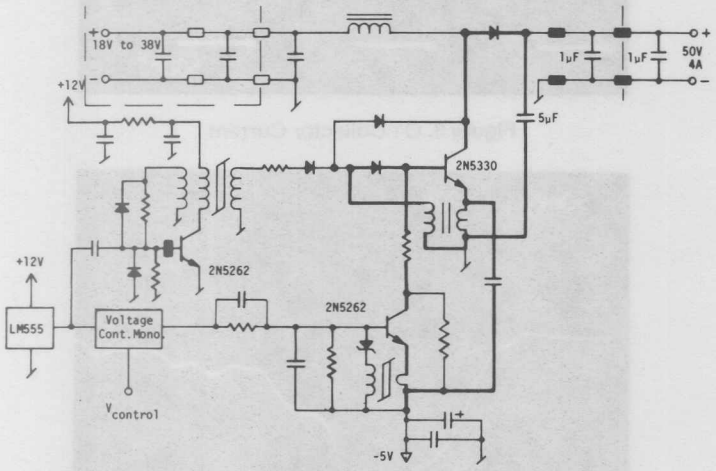


Figure 6. 300kHz Boost Converter

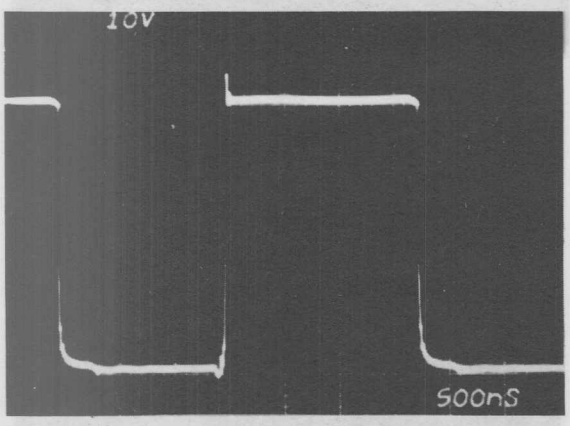


Figure 7. Q1 Collector Voltage

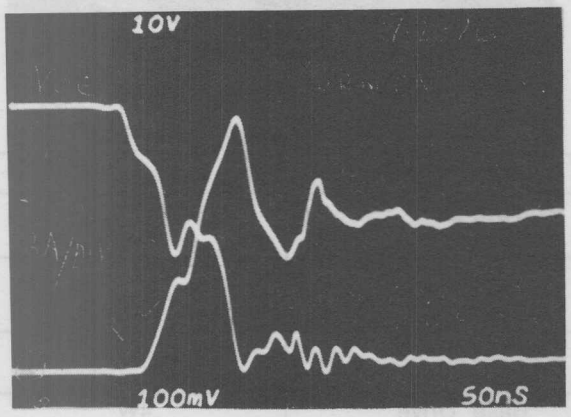


Figure 8. Q1 Turn-On Transition

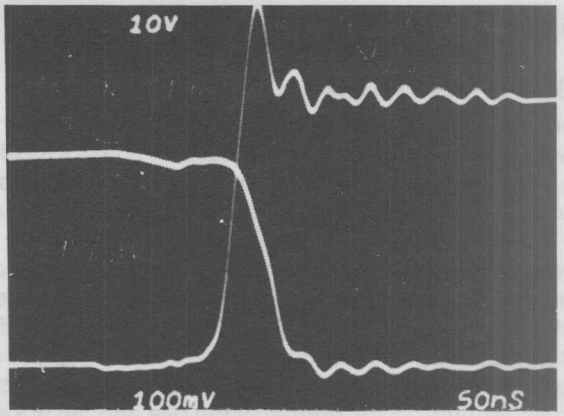


Figure 9. Q1 Turn-Off Transition

3. A Complete 300/600kHz Power Supply

At the completion of testing the aforementioned 300 kHz boost regulator breadboard, it was apparent that a power supply operating with a much higher than normal switching frequency could be built. Concurrently, a requirement had appeared for a satellite navigation receiver power supply that required minimum weight. The receiver had IF circuits operating in the range of 20 to 40kHz which were sensitive to μV signals, therefore, the power supply switching frequency had to be well above the IF frequencies.

Table II is a summary of the output requirements. (The input power was derived either from a pair of 12V lithium batteries or from a vehicle). The block diagram for the supply is given in Figure 10.

Two output converters were used to provide efficient operation during both nominal and standby when the load is much reduced. The main converter supplies 22W and the standby converter 1.8W.

The main power converter is a quasi-squarewave type running at 300kHz. As can be seen in Figure 11, the output circuit arrangement is quite conventional, except for the switching frequency and the component values. The transistors are being driven by the circuit shown in Figure 2. The collector voltage and current waveforms are shown in Figures 12, 13, 14 and 15. Converter efficiency was 85%.

In the main converter the feedback loop samples the +12V output. A concern for the regulation of outputs not sensed is usually raised when high frequency operation is considered; the assumption is that the regulation will degrade. That does *not* appear to be the case. The regulation envelopes for the +12, +5V, and -12V outputs are given in Figures 16, 17 and 18. The output voltages remain within the shaded areas for line, temperature and load variations. A worst case load profile was generated by placing all loads at maximum and then reduced one at a time to minimum. All loads were then placed at minimum and raised to maximum one at a time. This was done for every temperature, (-40° C to +100° C) and line variations of +22V to +28V. Note that 17W of the total 22W output is in the unsensed winding! The regulation is every bit as good as would be expected of a 20kHz converter.

The 1.8W standby converter is a dual-output buck-boost configuration shown in Figure 19. Figures 20, 21, 22 and 23

show the collector voltage and current waveforms. The current ringing at turn-on was eliminated by placing a ferrite bead on the collector load. One of the new power MOS FET's was used for the switch for simplicity and to gain experience with these devices. However, a bipolar device could just as well have been used. Of particular interest was the output regulation. This type of converter does not have the best multiple-ouput regulation performance even at low frequencies. The voltage regulation on the 5V output was ±2% with the loop sensing the 12V output.

Table II
Manpack Power Supply Output Requirements

Voltages	Min Load Current	Max Load Current	Regulation
+12V, Analog	.07	.14	±1%
+12V, Digital	.08	.16	±1%
+5V	1.7A	3.4A	±4%
-12V	.05	.1A	±4%
+12V, Standby	.05	.1A	±1%
+5V, Standby	.06	.12A	±4%
+18.5V	.1A	1.2A	±2%
+5V RAM	4mA	50mA	±4%

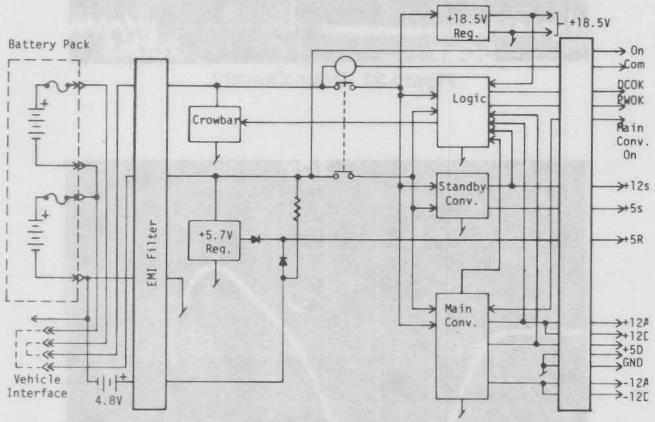


Figure 10. Manpack Power Supply Block Diagram

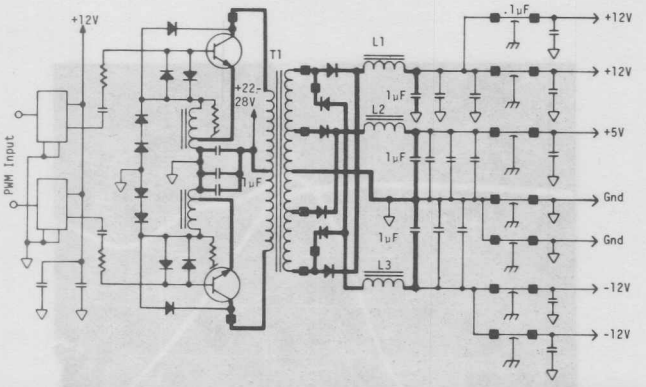


Figure 11. 300kHz Converter Output Circuit

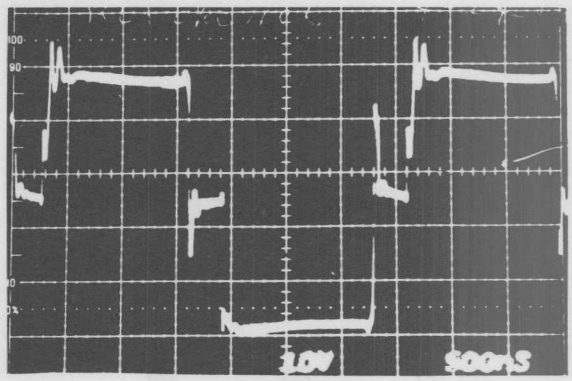


Figure 12. Collector Voltage

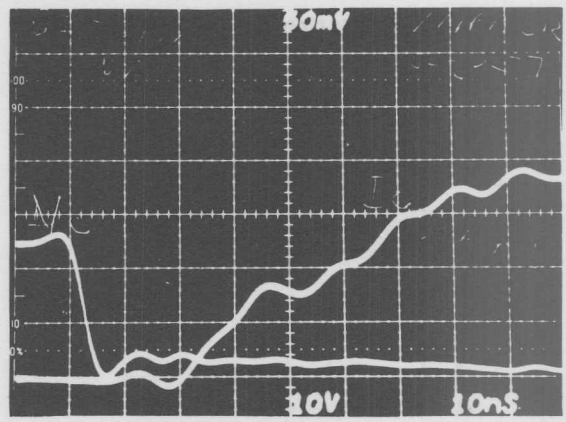


Figure 13. Turn-On Transition

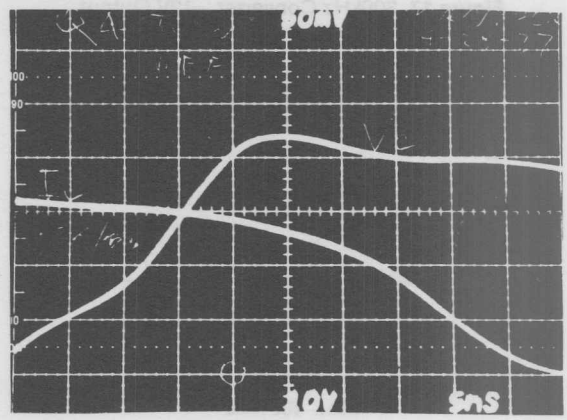


Figure 14. Turn-Off Transition

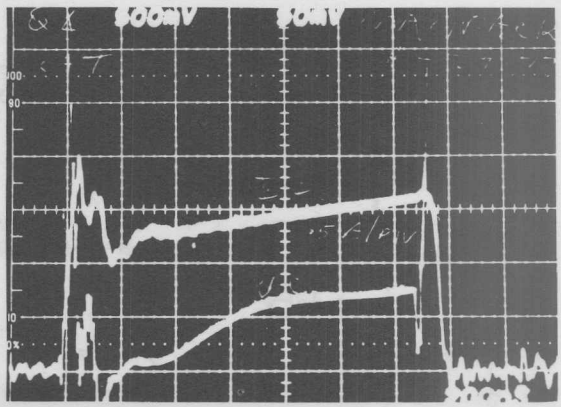


Figure 15. Collector Voltage & Current During Conduction

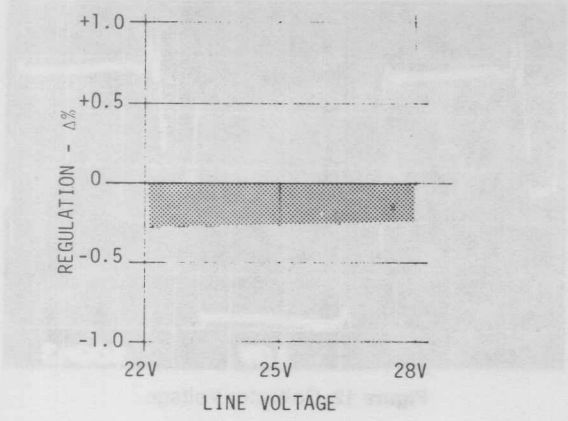


Figure 16. 300kHz Converter, +12V Output

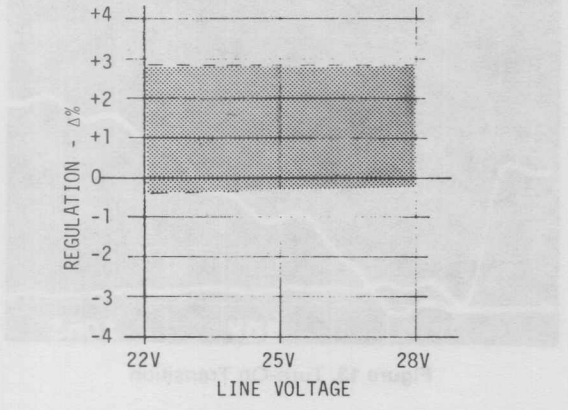


Figure 17. 300kHz Converter, -12V Output

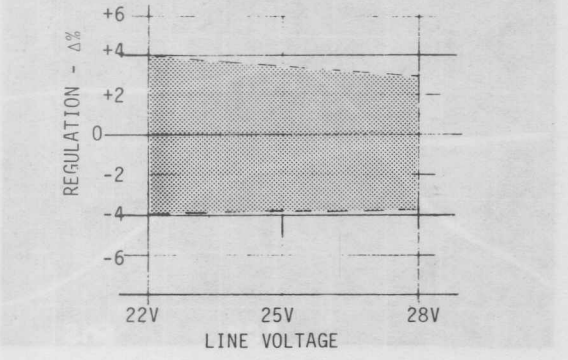


Figure 18. 300kHz Converter, +5V Output

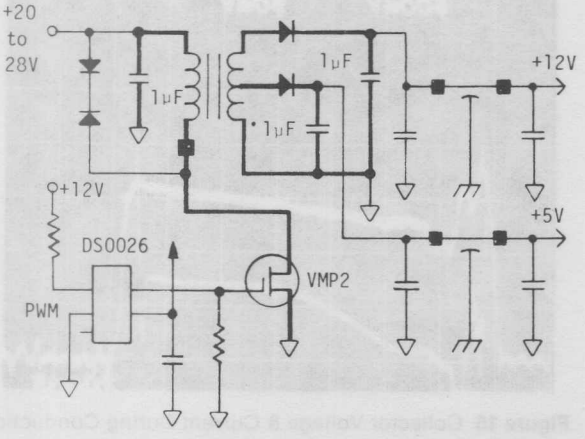


Figure 19. 600kHz Converter Output Circuit

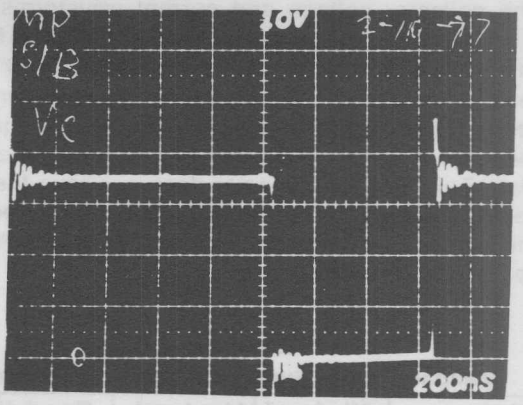


Figure 20. Drain Voltage

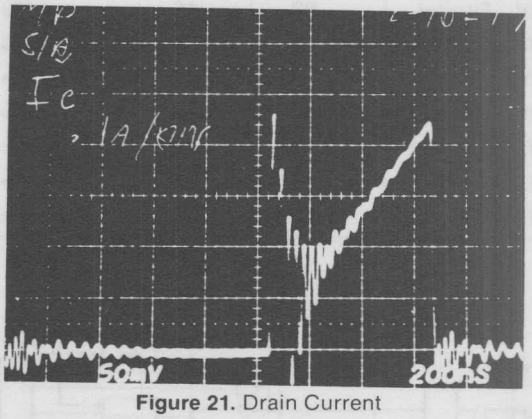


Figure 21. Drain Current

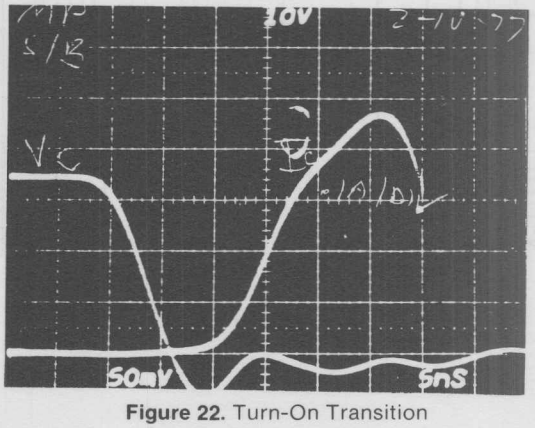


Figure 22. Turn-On Transition

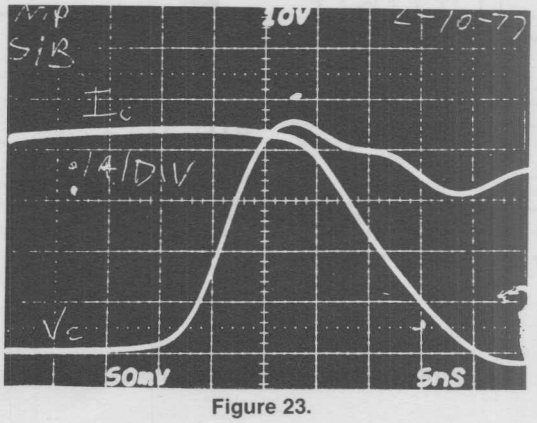


Figure 23.

CONCLUSION

Having gone through this exercise of selecting new topologies, components and layouts, one wonders if it's really worthwhile. Is the volume and weight reduced, is there any cost reduction, and can we do better in the immediate future?

Some of the pro and con arguments for these questions are summarized in Tables IX, X, and XI. The amount of volume reduction realized is very much a function of power output. From zero to 20 watts little is gained by going to high frequencies; from 20 to 100 watts the volume may be reduced by a factor of 1.5, and above 100 watts a factor of 3 or more may be obtainable. The actual size reduction achieved depends strongly on the power supply specifications. If, for example, a line voltage dropout of 50 or 100 ms must be accommodated, the size of the DC energy storage capacitors is so great that the operating frequency of the converter is relatively unimportant. On the other hand, in those applications where the line dropout requirement is very small and conduction cooling is provided, the size reduction can be dramatic.

The answer to the cost question is a definite maybe. There really have not been enough commercial switchers designed at these frequencies to know the relative value to the arguments in Table X, but if the cost of the MOSFETs and fast diodes can be reduced, the high frequency converters should be cheaper to build.

A final note of caution: Most designers find that their first effort at 200 kHz usually isn't much smaller than what they could built at 20 kHz! Don't be discouraged. It takes time to appreciate the differences and to exploit the possibilities of high frequencies. Usually by the second or third effort the performance advantages talked about here will begin to appear.

Table IX. Size/Volume Reduction Tradeoffs

PRO	CON
1. Transformers Smaller 2. RFI Filters Much Smaller 3. Capacitors Smaller	1. Heat Sinks No Smaller 2. Semiconductor Packages No Smaller 3. Auxillary Circuits No Smaller 4. Line Holdup Capacitors Only Slightly Smaller

Table X. Cost Tradeoffs

PRO	CON
1. Magnetics Cheaper 2. EMI Filters Cheaper 3. Filter Capacitors Cheaper 4. Power MOSFETs will be Competitive in Cost with Low Frequency Bipolar	1. Junction Diodes More Expensive 2. HF Bipolar Switches More Expensive 3. Shielding for RFI Required

Table XI. Expected Future Improvements

1. High Current, Low Voltage Film Capacitors
2. Lower Cost Low t_{rr} Diodes
3. More Practical Transformer Designs
4. A Good 300 KHz Modulator IC
5. Wide Variety of Low Cost Polar MOSFETs

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